Please enter the following amendments:

In the Specification:

Amend the second paragraph beginning at line 12 of page 6 and extending to line 24 of page 7 as follows:

Illustrated in FIG. 2 is a diagram of a portion of a configuration of the prefetch buffer 30 based upon different burst length support. In the illustrated form, a plurality of burst blocks or burst lines, such as burst lines 36, 38, 40, 42, 44 and 46, is provided. Burst lines 36 and 38 support eight word (i.e. thirty-two bit words) burst operation. Within each burst line, such as burst line 36 is a status field 48 and a predetermined number of data words in a data field 50. Prefetch buffer 30 is configured for eight word burst operation in each of burst lines 36 and 38, whereas prefetch buffer 30 is configured for four word burst operation in each of burst lines 40, 42, 44 and 46. Because there are two different sizes of burst lines, it is clear that the master is supporting at least two lengths of memory bursting, or conversely, that different bus masters support different burst lengths. It should be understood that the data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26 than the data from burst line ~~36~~ 38. The same is true with respect to the source of data in all of the other illustrated burst lines. The particular configuration of prefetch buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and the Burst Length signal. The Data Size signal determines the size of a single unit of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. In FIG. 2, the Data Size signal selects a data size being a word in length. Other data sizes such as multiple words or a byte could be indicated by the

Data Size signal. The Burst Length signal allows the use of different types of bus masters to be implemented in data processing system 10. For example, if the first master 12 only supports bursts of eight words in length and the second bus master 14 supports bursts of four words in length, the prefetch buffer configuration of FIG. 2 will support both of these bus masters. In contrast, previous systems would require separate storage elements with predetermined fixed configurations to separately support the two differing bus masters. It should be noted that in the illustrated portion of prefetch buffer 30 of FIG. 2, the buffer storage area is dynamically configurable, based on the requested accesses to be serviced. Thus, although the illustrated configuration contains two burst line buffers holding eight words each and four burst line buffers holding four words each, depending on the history and type of burst requests, the buffers may be dynamically configured into any combination of lengths as access requests are received. Dynamic configuration of the buffers may be based at least in part on the Data Size and Burst Length signals.

Amend the paragraph beginning at line 25 of page 7 and extending to line 12 of page 8 as follows:

Illustrated in FIG. 3 is an alternative configuration of a portion of prefetch buffer 30 for a non-bursting memory operation. In response to the Data Size signal and the Burst Length signal, the prefetch control circuitry adaptively configures the line size of the prefetch buffer 30. The Burst Length signal indicates that the bus master that is communicating a read request is not supporting a burst transaction for the requested data. This may be because of

the type of access or any of other various reasons. The buffer lines 52, 54, 56 and 58 each have a single data word attached to a status field. In addition, buffer lines 60 and 62 have two data words attached to a status field in response to the Data Size signal indicating a data size of two words. In each of buffer lines 52, 54, 56, ~~68~~ 58, 60 and 62 no data bursting is indicated by the Burst Length signal. Therefore, it should be noted that a variety of differing prefetch buffer configurations may be implemented in response to the prefetch control circuitry 32 receiving the Data Size signal and the Burst Length signal.

On page 8, amend the paragraph beginning at line 13 and extending to line 22 of page 9 as follows:

Illustrated in FIG. 4 is an illustration of a status field 64 that represents, by way of example only, any of the status fields illustrated in FIGs. 2 and 3. The status field 64 has an Address Tag Field or Tag Field, an Invalid Field or Invalid indicator, a Used Field or Used indicator, a Valid Field or Valid indicator, a Prefetched Field or Prefetched indicator, a Busy Bus Field or Busy Bus indicator and a Busy Fill Field or Busy Fill indicator. As was illustrated in FIGs. 3 and 4, the status field is associated with the smallest supported line size in the prefetch buffer 30. The Tag Field contains information that locates where in the prefetch buffer 30 a particular line of data is. The Invalid indicator denotes that the prefetch buffer 30 contains no valid data. In other words, the Invalid field indicates that a corresponding line of data in the prefetch buffer 30 is not valid. The Used indicator denotes that the prefetch buffer 30 contains valid data that has been provided to satisfy a bus burst type read. In other words, the Used field indicates that a corresponding line of data

in the prefetch buffer 30 has been provided in response to a previous burst read request. The Valid indicator denotes that the prefetch buffer 30 contains valid data that has been provided to satisfy a bus single type (i.e. non-burst) read. In other words, the Valid field indicates a corresponding line in the prefetch buffer 30 has been provided in response to a previous non-burst read request. The Prefetched indicator denotes that the prefetch buffer 30 contains valid data that has been prefetched to satisfy a potential future bus access. The Busy Bus indicator denotes that the prefetch buffer 30 is currently being used to satisfy a bus burst read initiated by one of the bus masters. The Busy Fill indicator denotes that the prefetch buffer 30 has been allocated to receive data from a memory and the memory access is still in progress. The memory access may have been initiated by a preftch operation performed by prefetch control circuitry 32 and not directly associated with an access request from one of the bus masters. These indicators in status field 64 are used to determine which line or lines in prefetch buffer 30 are selected as a replacement entry. Selection of which line or lines to be chosen as a replacement entry is made in a prioritized order of the indicators of status field in the order of Invalid, Used, Valid, Prefetched, Busy Bus and Busy Fill as illustrated in FIG. 4. Note that alternate embodiments may use different indicators than those illustrated in FIG. 4 or may combine or encode indicators in an alternate manner.

Amend the paragraph beginning at line 9 of page 10 and extending to line 19 of page 11 as follows:

Illustrated in FIGs. 6-8 is a flowchart 79 describing the operation of data processing system 10 and in particular the implementation 70 of prefetch control circuitry 32. In a step 80, a read access in initiated. The read request is received from one of the bus masters 12, 14 or 16 in a step 82 by memory controller 20. In a step 84 a decision is made whether the read request results in a hit in the prefetch buffer 30. This decision is made as a conventional tag comparison (not shown) in the memory controller 20. If a tag match results in a hit, a step 86 is followed wherein a read to the master is made from prefetch buffer 30. An end of the read access occurs in step 88. If a miss occurs, a step 90 is implemented. A determination is made within the memory controller 20 as to whether the Master Identification (ID) signal bus of the requesting master is allowed to reconfigure the prefetch buffer 30. Logic circuitry (not shown) determines which bus masters have reconfiguration capability. Alternate embodiments may allow for reconfiguration by any bus master and thus may omit the determination step 90. If the requesting bus master can reconfigure prefetch buffer 30, then a step 92 is implemented. Based on the data size attribute and the burst length attribute corresponding to the read access, a reconfiguration indicator is selectively asserted by the Adaptive Buffer Store Replacement logic 74. The reconfiguration indicator may take one of numerous forms. For example, the reconfiguration indicator may be a signal, a machine state, a logic state, a statically driven signal, a flag indicator, an externally supplied signal at an integrated circuit pin, etc. If the requesting bus master cannot reconfigure prefetch buffer 30, then the reconfiguration indicator is negated in a step 94 by the Adaptive Buffer Store Replacement logic 74. In either event, a step 96 is implemented wherein some or all of the status fields are checked for any invalid entry in the prefetch buffer 30. It should be noted that the term 'entry' is either an entire line, a

portion of a line, or more than one line. A determination is made in step 96 whether an invalid entry is found. If an invalid entry is found, the line(s) or portion of a line that was found to be invalid are marked in step 100 as a replacement entry. The portion of the line(s) that is marked depends upon the size of the entry to be replaced. One or more lines, or selection of at least a portion of a plurality of lines as a replacement entry may be performed, depending on the necessary capacity needed for the replacement data. After step 100, further steps to be described in connection with FIG. 8 are implemented.